

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: DeWitt, Jr. et al.	§	
	§	Group Art Unit: 2183
Serial No. 10/675,778	§	
	§	Examiner: Cody, Dillon J.
Filed: September 30, 2003	§	
	§	
For: Method and Apparatus for	§	
Counting Data Accesses and	§	
Instruction Executions that Exceed a	§	
Threshold Value in a Data Processing		
System		

Commissioner for Patents
P.O. Box 1450
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35525
PATENT TRADEMARK OFFICE
CUSTOMER NUMBER

APPEAL BRIEF (37 C.F.R. 41.37)

This brief is in furtherance of the Notice of Appeal, filed in this case on July 31, 2006.

A fee of \$500.00 is required for filing an Appeal Brief. Please charge this fee to IBM Corporation Deposit Account No. 09-0447. No additional fees are believed to be necessary. If, however, any additional fees are required, I authorize the Commissioner to charge these fees which may be required to IBM Corporation Deposit Account No. 09-0447. No extension of time is believed to be necessary. If, however, an extension of time is required, the extension is requested, and I authorize the Commissioner to charge any fees for this extension to IBM Corporation Deposit Account No. 09-0447.

REAL PARTY IN INTEREST

The real party in interest in this appeal is the following party: International Business Machines Corporation of Armonk, New York.

RELATED APPEALS AND INTERFERENCES

With respect to other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal, there are no such appeals or interferences.

STATUS OF CLAIMS

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application are: 1-25

B. STATUS OF ALL THE CLAIMS IN APPLICATION

1. Claims canceled: NONE
2. Claims withdrawn from consideration but not canceled: NONE
3. Claims pending: 1-25
4. Claims allowed: NONE
5. Claims rejected: 1-25
6. Claims objected to: NONE

C. CLAIMS ON APPEAL

The claims on appeal are: 1-25

STATUS OF AMENDMENTS

A Response after Final Rejection was not filed. Therefore, the claims on appeal herein are as presented in the Response to Office Action filed May 3, 2006 and finally rejected in the Final Office Action dated May 31, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

A. CLAIM 1 - INDEPENDENT

The subject matter of claim 1 is directed to a method in a data processing system for processing instructions. Responsive to receiving an instruction at a processor in the data processing system (**1300, Figure 13**, page 34, lines 12-13), it is determined whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator (**1302, Figure 13**, page 34, lines 13-20). Executions of the instruction are counted if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value (**1306, 1308, Figure 13**, page 35, lines 4-10).

B. CLAIM 9 - INDEPENDENT

The subject matter of claim 9 is directed to a method in a data processing system for processing instructions. An initial instruction is received at a processor in the data processing system (**1300, Figure 13**, page 34, lines 12-13). The initial instruction indicates that counting execution of a subsequent instruction occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction (**1306, 1308, Figure 13**, page 35, lines 4-10). Executions of the subsequent instruction are counted if the time to execute the subsequent instruction exceeds the threshold value (**1310, Figure 13**, page 35, line 19 to page 36, line 12).

C. CLAIM 11 - INDEPENDENT

The subject matter of claim 11 is directed to a method in a data processing system for processing data. Responsive to a request to access data (**1300, Figure 13**, lines 12-13), it is determined whether an indicator is associated with the data, wherein a threshold value is located in the indicator (**1302, Figure 13**, page 34, lines 13-20). Access to the data is counted if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value (**1306, 1308, Figure 13**, page 35, lines 4-10, see also page 36, lines 13-25).

D. CLAIM 16 - INDEPENDENT

The subject matter of claim 16 is directed to a data processing system for processing instructions. Responsive to receiving an instruction at a processor (**102, Figure 1, 210, Figure 2**, page 12, lines 11-13, page 14, lines 17-21) in the data processing system (**100, Figure 1**, page 12, lines 2-6), a determining means (**214, Figure 2**, page 15, lines 4-9) determines whether an indicator (**510, 512, 514, Figure 5**, page 27, lines 1-15) is associated with the instruction, wherein a threshold value is located in the indicator (page 27, lines 10-12). Counting means (**241-242, Figure 2**, page 21, lines 10-13) counts executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value.

E. CLAIM 19 - INDEPENDENT

The subject matter of claim 19 is directed to a data processing system for processing instructions. Receiving means (**218, Figure 2**, page 15, lines 4-9) receives an initial instruction at a processor (**102, Figure 1, 210, Figure 2**, page 12, lines 11-13, page 14, lines 17-21) in the data processing system (**100, Figure 1**, page 12, lines 2-6). The initial instruction indicates that counting execution of a subsequent instruction occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction. Counting means (**241-242, Figure 2**, page 21, lines 10-13) counts executions of the subsequent instruction if the time to execute the subsequent instruction exceeds the threshold value.

F. CLAIM 21 - INDEPENDENT

The subject matter of claim 21 is directed to a data processing system for processing data. Responsive to a request to access data, determining means (**216, Figure 2**, page 24, line 26-page 25, line 4) determines whether an indicator (**510, 512, 514, Figure 5**, page 27, lines 1-15) is associated with the data, wherein a threshold value is located in the indicator (page 27, lines 10-12). Counting means (**241-242, Figure 2**, page 21, lines 10-13) counts access to the data if the

indicator is associated with the data and if a time needed to access the data exceeds the threshold value.

G. CLAIM 23 - INDEPENDENT

The subject matter of claim 23 is directed to a computer program product in a computer readable, recordable-type medium for processing instructions. The computer program product includes first instructions for receiving an instruction at a processor in the data processing system responsive to determining whether an indicator is associated with the instruction (**1300, Figure 13**, page 34, lines 12-13), wherein a threshold value is located in the indicator (**1302, Figure 13**, page 34, lines 13-20). The computer program product also includes second instructions for counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value (**1306, 1308, Figure 13**, page 35, lines 4-10).

H. CLAIM 24 - INDEPENDENT

The subject matter of claim 24 is directed to a computer program product in a computer readable, recordable-type medium for processing instructions. The computer program product includes first instructions for receiving an initial instruction at a processor in the data processing system (**1300, Figure 13**, page 34, lines 12-13), wherein the initial instruction indicates that counting execution of a subsequent instruction occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction (**1306, 1308, Figure 13**, page 35, lines 4-10). The computer program product also includes second instructions for counting executions of the subsequent instruction if the time to execute the subsequent instruction exceeds the threshold value (**1310, Figure 13**, page 35, line 19 to page 36, line 12).

I. CLAIM 25 - INDEPENDENT

The subject matter of claim 25 is directed to a computer program product in a computer readable, recordable-type medium for processing data. The computer program product includes

first instructions for determining whether an indicator is associated with the data, responsive to a request to access data (**1300, Figure 13**, lines 12-13), wherein a threshold value is located in the indicator (**1302, Figure 13**, page 34, lines 13-20). The computer program product also includes second instructions for counting access to the data if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value (**1306, 1308, Figure 13**, page 35, lines 4-10, see also page 36, lines 13-25).

J. CLAIM 3 - DEPENDENT

The subject matter of claim 3, which depends from claim 1, recites that the threshold value is a three bit value located in the indicator (page 34, lines 21-25).

GROUND OF REJECTION TO BE REVIEWED ON APPEAL

A. GROUND OF REJECTION 1 (Claims 1-2 and 4-25)

Claims 1-2 and 4-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Davidson et al., Method and System for Providing Temporal Threshold Support During Performance Monitoring of a Pipelined Processor, U.S. Patent No. 6,446,029 (September 3, 2002) .

B. GROUND OF REJECTION 2 (Claim 3)

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Davidson et al., Method and System for Providing Temporal Threshold Support During Performance Monitoring of a Pipelined Processor, U.S. Patent No. 6,446,029 (September 3, 2002).

ARGUMENT

A. GROUND OF REJECTION 1 (Claims 1-2 and 4-25)

Claims 1-2 and 4-25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Davidson et al., Method and System for Providing Temporal Threshold Support During Performance Monitoring of a Pipelined Processor, U.S. Patent No. 6,446,029 (September 3, 2002) (hereinafter “Davidson”).

In rejecting the claims, the Examiner states as follows with respect to claim 1:

As per claim 1, Davidson discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction (Col. 7 line 64-Col. 8 line 32), wherein a threshold value is located in the indicator (Fig. 5B threshold registers 521-525); and counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value (Col. 8 lines 61-65). *The examiner asserts that, as described in col. 7 line 64 – col. 8 line 32, the instruction tag and the threshold value registers collectively comprise the “indicator”. As such, the indicator contains the threshold values.*

Final Office Action dated May 31, 2006, pages 2 and 3.

Claim 1 of the present application is as follows:

1. A method in a data processing system for processing instructions, the method comprising:
responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator; and
counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value.

A prior art reference anticipates a claimed invention under 35 U.S.C. § 102 only if every element of the claimed invention is identically shown in that single prior art reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir.

1990). All limitations of a claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983).

Appellants respectfully submit that Davidson does not identically show every element of the claimed invention arranged as they are in the claims; and, accordingly, does not anticipate the claims. With respect to claim 1, in particular, Appellants respectfully submit that Davidson does not teach or suggest “responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator”; and also does not teach or suggest “counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value”.

Davidson is directed to a mechanism for monitoring performance of an instruction pipeline. In particular, Davidson discloses monitoring instructions that are to execute within specified threshold time intervals, and counts occurrences of exceeding the threshold intervals.

In rejecting the claims, the Examiner refers to threshold registers 521-525 in Fig. 5B of Davidson as being a disclosure of a threshold value located in an indicator, and to col. 8, lines 61-65 of Davidson as disclosing counting executions of an instruction if an indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value. Col. 8, lines 59-66 of Davidson is as follows:

Threshold **520** monitors the stage completion signals and compares the time intervals of each pipeline instruction stage with threshold values stored in threshold registers **521-525**. If an instruction pipeline stage requires more time to complete than indicated by its corresponding threshold value, then threshold **520** asserts a threshold event signal **526** that is collected by an event counter or multiple event counters **530** in the performance monitor.

Appellants respectfully disagree that the above recitation in Davidson discloses or suggests “counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value” as recited in claim 1. At best, the above recitation may disclose counting “a threshold event signal” which is asserted “[i]f an

instruction pipeline stage requires more time to complete than indicated by its corresponding threshold value”. Counting threshold event signals which are asserted if an instruction pipeline stage requires more time to complete than indicated by corresponding threshold values is not the same as counting executions of an instruction, and is certainly not the same as “counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value” as required by claim 1. Davidson simply does not disclose, in Col. 8, lines 61-65 or elsewhere, “counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value”, and does not anticipate claim 1.

Appellants also disagree that Davidson discloses or suggests “responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator” as recited in claim 1. In rejecting the claim, the Examiner asserts that the instruction tag described in Col. 7, line 64-Col. 8, line 32 of Davidson and the threshold value registers 521-525 described in Col. 8, lines 61-65 of Davidson (reproduced above) collectively comprise the “indicator” of claim 1, and as such, the indicator includes the threshold values. Appellants respectfully disagree with such an interpretation of Davidson.

Col. 7 line 64-Col. 8 line 32 of Davidson is as follows:

As an instruction is fetched, a single instruction may be selected and marked (or tagged). As the marked instruction flows through each pipeline unit representing a stage of the instruction pipeline, each pipeline unit signals its completion of the processing for the marked instruction by asserting a stage complete signal, such as signal 510. Performance monitor 500 collects the signals and makes the signals available to logic analysis software or performance analysis software.

Alternatively, each pipeline unit may signal its completion of any instruction without the requirement that the instruction has been previously tagged.

at If only a single marked instruction may proceed through the instruction pipeline any given time, then the instruction may be simply marked with a single bit. If multiple instructions may be marked, then a tag consisting of multiple bits may identify marked instructions.

Instructions may be marked based on a variety of selection mechanisms, each of which may be under the control of the performance monitor. An instruction may be selected at random, in which case the performance monitor may capture the instruction address after the instruction has been randomly selected, e.g., by receiving instruction address 509 from fetch unit 501. An instruction may be selected based on a general

category of its instruction type, such as any store instruction. A specific type of instruction may be selected, such as a load instruction that uses particular registers. As another alternative, an instruction may be selected based on its instruction address, which provides functionality for a debugging program to store specific instructions at specific addresses and then to allow the processor to execute the instructions without setting interrupts or traps. The above list merely provides some examples and should not be considered an exhaustive list of potential instruction selection mechanisms.

In Davidson, threshold registers 521-525 store threshold values, whereas instructions are selected and marked for monitoring. The threshold values are not located in an indicator associated with an instruction as required by claim 1, and there is nothing in the above paragraphs or anywhere else in Davidson that would suggest or support such an interpretation.

Furthermore, claim 1 specifically recites “responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator.” Even if the instruction tag and the threshold value registers in Davidson can somehow be construed as collectively comprising an indicator, there is never any determination made in Davidson as to whether the threshold registers are associated with instructions which flow through the pipeline units in Davidson which would appear to be necessary if the indicator includes the threshold registers. The threshold registers are always present in Davidson and making such a determination would be meaningless at the very least.

Therefore, Davidson also does not disclose or suggest “responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator” as recited in claim 1, and does not anticipate claim 1 for this reason as well.

For at least all the above reasons, claim 1 is not anticipated by Davidson and patentably distinguishes over Davidson in its present form.

Claims 2 and 4-8 depend from and further restrict claim 1 and are also not anticipated by Davidson, at least by virtue of their dependency.

Independent claims 9, 11, 16, 19, 21 and 23-25 are also not anticipated by Davidson for similar reasons as discussed above with respect to claim 1. Claims 10, 12-15, 17-18, 20 and 22 depend from and further restrict one of claims 9, 11, 16, 19 and 21; and are also not anticipated by Davidson, at least by virtue of their dependency.

Claims 1-2 and 4-25, accordingly, are not anticipated by Davidson and patentably distinguish over Davidson, and it is respectfully requested that the Board reverse the Examiner's Final Rejection of those claims.

B. GROUND OF REJECTION 2 (Claim 3)

Claim 3 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Davidson et al., Method and System for Providing Temporal Threshold Support During Performance Monitoring of a Pipelined Processor, U.S. Patent No. 6,446,029 (September 3, 2002).

Claim 3 depends from claim 1, and recites that the threshold value is a three bit value located in the indicator. In rejecting the claim, the Examiner acknowledges that Davidson fails to disclose the subject matter of claim 3, but contends that it would have been obvious to one of ordinary skill in the art at the time of invention to have located the threshold values inside the indicator for the benefit of reduced logic. The Examiner also asserts that using three bits to represent the threshold value would be obvious because "a small amount of logic is needed to represent the value and up to eight different values can be produced". Appellants respectfully disagree with the Examiner's conclusions.

A *prima facie* case of obviousness must be supported by some teaching, suggestion, or incentive contained in the prior art which would have led one of ordinary skill in the art to make the claimed invention. The Examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The requirements for establishing a *prima facie* case of obviousness include the requirements that the Examiner explain in detail why an artisan would have found the claimed invention obvious in light of the teachings of the cited prior art, and that the Examiner provide a showing that it is the prior art and not the Applicants' own disclosure that teaches the modification asserted by the Examiner.

Davidson discloses only that threshold values are stored in threshold registers. Davidson contains no disclosure or suggestion of any kind that threshold values can or should be located in an indicator that is associated with an instruction, and certainly does not disclose or suggest that the threshold value is a three bit value located in the indicator. Only the present application contains such a disclosure and Appellants submit that the Examiner is using hindsight based on

Appellants' own disclosure to modify Davidson in an effort to achieve the present invention. Appellants submit that the Examiner has not established a *prima facie* case of obviousness in rejecting claim 3, and that claim 3 patentably distinguishes over Davidson in its own right as well as by virtue of its dependency from claim 1.

Claim 3, accordingly, is not unpatentable over Davidson, and it is respectfully requested that the Board reverse the Examiner's Final Rejection of that claim.

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CLAIMS APPENDIX

The text of the claims involved in the appeal are:

1. A method in a data processing system for processing instructions, the method comprising:
responsive to receiving an instruction at a processor in the data processing system,
determining whether an indicator is associated with the instruction, wherein a threshold value is
located in the indicator; and
counting executions of the instruction if the indicator is associated with the instruction and
if a time for executing the instruction exceeds the threshold value.
2. The method of claim 1, wherein the counting step comprises:
determining whether the time to execute the instruction exceeds the threshold value;
generating, by an instruction cache, a signal indicating that executions of the instruction are to be
counted if a determination is made that the time for executing the instruction exceeds the threshold
value;
receiving the signal generated by the instruction cache at a performance monitor unit; and
incrementing a counter in the performance monitor unit each time the instruction is
executed in response to receiving the signal from the instruction cache.
3. The method of claim 1, wherein the threshold value is a three bit value located in the
indicator.
4. The method of claim 1, wherein the indicator is located in a shadow memory.

5. The method of claim 1, wherein the instruction is received in a bundle and wherein the indicator comprises at least one spare bit in a field in the bundle.

6. The method of claim 1, wherein the counting step comprises:

determining whether the time to execute the instruction exceeds the threshold value;
generating, by an instruction cache, a signal indicating an interrupt is present if a determination is made that the time for executing the instruction exceeds the threshold value;

receiving the signal generated by the instruction cache at an interrupt unit; and

executing code, by the interrupt unit, to count each execution of the instruction.

7. The method of claim 6, wherein the code also gathers information from a call stack for the instruction.

8. The method of claim 1, wherein the threshold is a number of clock cycles.

9. A method in a data processing system for processing instructions, the method comprising:

receiving an initial instruction at a processor in the data processing system, wherein the initial instruction indicates that counting execution of a subsequent instruction occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction; and

counting executions of the subsequent instruction if the time to execute the subsequent instruction exceeds the threshold value.

10. The method of claim 9, wherein the counting step comprises:

determining whether the time to execute the subsequent instruction exceeds the threshold value;

generating, by an instruction cache, a signal indicating that each execution of the subsequent instruction is to be counted if a determination is made that the time for executing the subsequent instruction exceeds the threshold value;

receiving the signal generated by the instruction cache at a performance monitor unit; and
incrementing a counter in the performance monitor unit each time the subsequent instruction is executed in response to receiving the signal from the instruction cache.

11. A method in a data processing system for processing data, the method comprising:

responsive to a request to access data, determining whether an indicator is associated with the data, wherein a threshold value is located in the indicator; and

counting access to the data if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value.

12. The method of claim 11, wherein the counting step comprises:

generating an exception if the indicator is associated with the data and if the time to access the data exceeds the threshold value.

13. The method of claim 11, wherein the counting step comprises:

determining whether the time to access the data exceeds the threshold value;

generating, by a data cache, a signal indicating that accesses of the data are to be counted if a determination is made that the time for accessing the data exceeds the threshold value;

receiving the signal generated by the data cache at a performance monitor unit; and

incrementing a counter in the performance monitor unit each time the data is accessed in response to receiving the signal from the data cache.

14. The method of claim 11, wherein the counting step comprises:

determining whether the time to access the data exceeds the threshold value;

generating, by a data cache, a signal indicating an interrupt is present if a determination is made that the time for accessing the data exceeds the threshold value;

receiving the signal generated by the data cache at an interrupt unit; and

executing code, by the interrupt unit, to count accesses of the data.

15. The method of claim 11, wherein the data is located in a memory location.

16. A data processing system for processing instructions, the data processing system comprising:

determining means, responsive receiving an instruction at a processor in the data processing system, for determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator; and

counting means for counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value.

17. The data processing system of claim 16, wherein the counting means comprises:

determining means for determining whether the time to execute the instruction exceeds the threshold value;

generating means for generating, by an instruction cache, a signal indicating that executions of the instruction are to be counted if a determination is made that the time for executing the instruction exceeds the threshold value;

receiving means for receiving the signal generated by the instruction cache at a performance monitor unit; and

incrementing means for incrementing a counter in the performance monitor unit each time the instruction is executed in response to receiving the signal from the instruction cache.

18. The data processing system of claim 16, wherein the counting means comprises:

determining means for determining whether the time to execute the instruction exceeds the threshold value;

generating means for generating, by an instruction cache, a signal indicating an interrupt is present if a determination is made that the time for executing the instruction exceeds the threshold value;

receiving means for receiving the signal generated by the instruction cache at an interrupt unit; and

executing means for executing code, by the interrupt unit, to count each execution of the instruction.

19. A data processing system for processing instructions, the data processing system comprising:

receiving means for receiving an initial instruction at a processor in the data processing system, wherein the initial instruction indicates that counting execution of a subsequent instruction occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction; and

counting means for counting executions of the subsequent instruction if the time to execute the subsequent instruction exceeds the threshold value.

20. The data processing system of claim 19, wherein the counting means comprises:

determining means for determining whether the time to execute the subsequent instruction exceeds the threshold value;

generating means for generating, by an instruction cache, a signal indicating that each execution of the subsequent instruction is to be counted if a determination is made that the time for executing the subsequent instruction exceeds the threshold value;

receiving means for receiving the signal generated by the instruction cache at a performance monitor unit; and

incrementing means for incrementing a counter in the performance monitor unit each time the subsequent instruction is executed in response to receiving the signal from the instruction cache.

21. A data processing system for processing data, the data processing system comprising:
- determining means, responsive to a request to access data, for determining whether an indicator is associated with the data, wherein a threshold value is located in the indicator; and
- counting means for counting access to the data if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value.
22. The data processing system of claim 21, wherein the counting means comprises:
- generating means for generating an exception if the indicator is associated with the data and if the time to access the data exceeds the threshold value.
23. A computer program product in a computer readable, recordable-type medium for processing instructions, the computer program product comprising:
- first instructions for receiving an instruction at a processor in the data processing system, responsive to determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator; and
- second instructions for counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value.
24. A computer program product in a computer readable, recordable-type medium for processing instructions, the computer program product comprising:
- first instructions for receiving an initial instruction at a processor in the data processing system, wherein the initial instruction indicates that counting execution of a subsequent instruction

occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction; and

second instructions for counting executions of the subsequent instruction if the time to execute the subsequent instruction exceeds the threshold value.

25. A computer program product in a computer readable, recordable-type medium for processing data, the computer program product comprising:

first instructions for determining whether an indicator is associated with the data, responsive to a request to access data, wherein a threshold value is located in the indicator; and

second instructions for counting access to the data if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value.

EVIDENCE APPENDIX

There is no evidence to be presented.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings.